said first areal size being larger than said second areal size such that said first breakdown voltage is larger than said second breakdown voltage.

2. Please add the following claims:

9. (Newly Added) A semiconductor arrangement as recited in claim 3, wherein said protection diode is a pn junction diode.

10. (Newly Added) A semiconductor arrangement as recited in claim 1, further comprising a channel stopper between said second diffusion region (45) and said second buried layer, wherein said channel stopper further reduces said second breakdown voltage relative to said first breakdown voltage.

Remarks

I. Status of the Claims

Upon entry of the present amendment, claims 1-5 and 9-10 are pending in the present application. Claim 1 is the independent claim, and claims 9-10 are newly added.

II. Submission of Substitute Specification

A substitute specification is enclosed herewith to overcome the objections to the specification noted on page 2 of the Office Action. A marked version showing the changes to the specification as filed is also enclosed.

III. Proposed Drawing Changes

The proposed changes to Figs. 3i and 3m are submitted in handwritten red ink. These changes are in response to informalities recited on page 2 of the Office Action. These changes add no new matter. Upon approval of these changes, formal drawings including the proposed changes will be submitted.

IV. Rejection Under 35 USC § 102(b)

The Office rejects claims 1 –5 under 35 USC § 102(e) in view of *Zambrano* (U.S. Patent 5,300,451). For at least the reasons set forth below, it is respectfully submitted that these claims are allowable over the cited reference.

To properly establish a *prima facie* case of anticipation, *all* of the claimed elements must be found in the prior art. It follows, therefore, that if a *single* claimed element is not found in the prior art, a *prima facie* case of anticipation cannot properly be established.

Claim 1 includes the limitations of:

a first diffusion region (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a ***first areal size*** *for defining a first breakdown voltage;*

a second diffusion region (45) in said second portion of said substrate layer (13), being of said second conductivity type and having a ***second areal size*** *for defining a second breakdown voltage;*

said first areal size being larger than said second areal size such that said first breakdown voltage is larger than said second breakdown voltage.

While the reference to *Zambrano* does disclose having the distance D of the power transistor of Fig. 1 of the reference being less than the distance L of the diode of Fig.1, which results in a lower breakdown voltage of the diode compared to the transistor, the reference does not teach nor suggest the claimed first and second areal sizes or the differential in the areal sizes as set forth in claim 1. (Please refer to Fig.1 and column 3, lines 10-30 of the reference to *Zambrano* for support for the above assertions.)

Because the reference to *Zambrano* lacks at least one of the claimed elements of independent claim 1, it cannot serve to establish a *prima facie* case of anticipation. As such, claim 1 and the claims that depend therefrom are believed to be allowable over the applied art. Allowance is earnestly solicited.

While newly added claim 10 further defines claim 1, and is therefore allowable for at least the reasons set forth above, it is noted that this claim is also distinguished over the applied art as including the limitation of:

"...a channel stopper between said second diffusion region (45) and said second buried layer, wherein said channel stopper further reduces said second breakdown voltage relative to said first breakdown voltage."

It is respectfully submitted that this limitation is neither taught nor suggested by the applied reference to *Zambrano*. As such, claim 10 is allowable thereover for at least this reason as well.

Conclusion

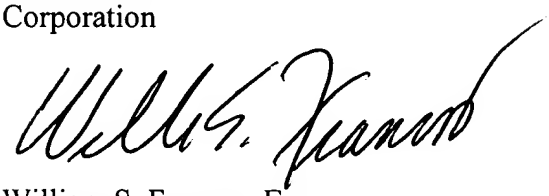
In view of the foregoing, it is respectfully requested that all objections and rejections be withdrawn. Allowance of all pending claims is earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact William S. Francos, Esq. (Reg. No. 38,456) at (610) 375-3513 to discuss these matters.

Except as otherwise stated in the previous Remarks, applicant notes that each of the amendments have been made to place the claims in better form for U.S. practice or to clarify the meaning of the claims; and not to distinguish the claims from applied art, otherwise narrow the scope, or to comply with other statutory provisions. Applicant reserves all entitled rights under the Doctrine of Equivalents.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies to charge payment or credit any overpayment to Deposit Account Number 50-0238 for any additional fees under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17.

Respectfully submitted on behalf of:
Philips Electronics North America Corporation



William S. Francos, Esq.
Reg. No. 38,456

VOLENTINE FRANCOS, P.L.L.C.
12200 SUNRISE VALLEY DRIVE
SUITE 150
RESTON, VA 20191
Tel.: (703) 715-0870
Fax.: (703) 715-0877

Marked Version Showing Changes to the Claims

1. (Once Amended) A semiconductor arrangement comprising:

- a substrate having a substrate layer (13) with an upper surface and a lower surface, the substrate layer (13) being of a first conductivity type;
- a first buried layer (12) in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer (13), and a second buried layer (12) in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer (13);
- a first diffusion region (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a first areal size [a first distance to said first buried layer (12)] for defining a first breakdown voltage [between said first diffusion region (26) and said first buried layer (12)];
- a second diffusion region (45) in said second portion of said substrate layer (13), being of said second conductivity type and having [a second distance to said first buried layer (12)] a second areal size for defining a second breakdown voltage [between said second diffusion region (45) and said first buried layer (12)]; and
- said first areal size [distance] being larger than said second areal size [distance] such that said first breakdown voltage is larger than said second breakdown voltage.

MARKED VERSION SHOWING CHANGES TO SPECIFICATION

Protection Diode for Improved Ruggedness of a Radio Frequency Power Transistor and Self-Defining Method to Manufacture Such Protection Diode

Field of the Invention

The present invention relates to a semiconductor arrangement with a protection diode for improved ruggedness of a radio frequency power transistor and self-defining method to manufacture such protection diode as defined in the outset of claim 1.

Background of the Invention

Radio frequency (RF) power transistors are used e.g. for mobile communication devices in the frequency range from 900 MHz to 2 GHz. Failure of RF power transistors can occur due to a mismatch of the load impedance (e.g. an antenna) and the output impedance of the transistor. Due to the impedance mismatch the voltage between base and collector of the RF transistor may increase above the level where breakdown occurs and the transistor becomes damaged. A protection diode connected between collector and emitter will prevent breakdown of the transistor by providing a lower breakdown voltage for the diode. Such a device is known from US 5751052, which shows a transistor integrated with a Zener diode as protection diode. In Figure 2 of US 5751052 a cross-sectional view of a device comprising a transistor and a protection Zener diode is shown. During the manufacturing of a device according to this prior art, the construction of the Zener diode requires additional processing steps. As known to persons skilled in the art of semiconductor technology, such steps comprise the formation of precisely defined lateral diffusion zones for which the respective depth must also be defined precisely.

Therefore, the formation of a Zener diode disadvantageously contributes to the manufacturing time and costs of the device. Moreover, the formation of a Zener diode may be prohibited in some types of power transistor device due to restrictions imposed by the technology. For example, in a double poly-Si process for bipolar devices as known in the art, formation of a Zener diode connected to a RF power transistor is not feasible.

Summary of the Invention

It is an object of the present invention to provide a bipolar device comprising a RF power transistor and a protection diode and a method to manufacture such a bipolar device in a double poly-Si process.

The present invention relates to a semiconductor arrangement comprising: a substrate having a substrate layer with an upper surface and a lower surface, the substrate layer being of a first conductivity type; a first buried layer in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer, and a second buried layer in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer; a first diffusion region in said first portion of said substrate layer, being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer for defining a first breakdown voltage between said first diffusion region and said first buried layer; a second diffusion region in said second portion of said substrate layer, being of said second conductivity type and having a second distance to said second buried layer for defining a second breakdown voltage between said second diffusion region and said second buried layer; said first distance being larger than said second distance such that said first breakdown voltage is larger than said second breakdown voltage.

Moreover, the present invention relates to the arrangement as described above, wherein said first diffusion region is a base of a bipolar transistor and said first buried layer is a collector of said bipolar transistor.

Also, the present invention relates to the aforementioned arrangement, wherein said second diffusion region is an anode of a protection diode and said second buried layer is a cathode of said protection diode.

Furthermore, the present invention relates to the aforementioned arrangement, wherein said first buried layer is connected to said second buried layer, and said first and second buried layers are manufactured in the same step.

Also, the present invention relates to the arrangement as defined above, further comprising a channel stopper region in said second portion of said substrate layer; the channel stopper region being of said first conductivity type, for electrically isolating said second portion of said substrate layer within the substrate, wherein said channel stopper region is arranged to extend substantially as an extended channel stopper region in between said second diffusion region and said second buried layer, for reducing said second breakdown voltage.

The present invention relates to a method of manufacturing a semiconductor arrangement, comprising the steps of:

- providing a substrate with a substrate layer with an upper surface and a lower surface, the substrate layer being of a first conductivity type, a first buried layer being

provided in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer, and a second buried layer being provided in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer;

- diffusing a first diffusion region in said first portion of said substrate layer, being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer for defining a first breakdown voltage between said first diffusion region and said first buried layer;

- diffusing a second diffusion region in said second portion of said substrate layer, being of said second conductivity type and having a second distance to said second buried layer for defining a second breakdown voltage between said second diffusion region and said second buried layer;

said first distance being larger than said second distance such that first breakdown voltage is larger than said second breakdown voltage.

Moreover, the present invention relates to the method described above, wherein said first and second diffusion regions are formed by depositing, in a single manufacturing step, a first poly-silicon layer in a first area in said first portion and a second poly-silicon layer in a second area in said second portion, and diffusing said first and second diffusion regions from said first and second poly-silicon layers, respectively, in a single annealing step, said first area being smaller than said second area.

Furthermore, the present invention relates to the aforementioned method, further comprising the step of forming by ion-implantation a channel stopper region in said second portion of said substrate layer ; the channel stopper regions being of said first conductivity type, for electrically isolating said second portion of said substrate layer within the substrate, wherein said channel stopper region is formed by ion-implantation as an extended channel stopper region in between said second diffusion region and said second buried layer, for reducing said second breakdown voltage.

According to the present invention the formation of the protection diode does not require any additional processing steps (e.g., deposition, implantation, masking and etching) in comparison with the processing steps required to construct a separate RF power transistor. The protection diode is formed within the same processing steps as the power transistor. Moreover, the method of the present invention is self-defining: i.e., any variations occurring during the processing steps will influence the electrical (and physical) properties of both power transistor and protection diode in a similar way. Under these circumstances the

breakdown voltage of the protection diode will always be lower than the detrimental breakdown voltage of the transistor.

Summary of the Invention

Below, the invention will be explained with reference to some drawings, which are intended for illustration purposes only and not to limit the scope of protection as defined in the accompanying claims.

Figure 1 shows a schematic, prior art illustration of a circuit comprising a RF power transistor and protection diode;

Figure 2 shows schematically a layout in plane view for a device comprising a RF power transistor and protection diode according to the present invention;

Figures 3a – 3m show schematically cross-sectional views of the transistor part of the device after successive processing steps according to the present invention;

Figures 4a and 4b show cross-sectional areas of the protection diode in two respective preferred embodiments after the step of metallization.

Detailed Description of the Invention

Figure 1 shows a schematic illustration of a prior art circuit comprising a RF power transistor and protection diode. In the circuit 1 of Figure 1, the RF power transistor 2 is shown comprising a base 3, an emitter 4 and a collector 5. The RF power transistor 2 is in a configuration, known in the art as a common emitter configuration, where emitter 4 and the substrate region 6 (not shown) are at electrical ground level. Between emitter 4 and collector 5 there is a parasitic capacitance 7 in series with a resistance 8. Parallel to the parasitic capacitance 7 and resistance 8 a protection diode 9 between collector 5 and emitter 4 is created in the manufacturing process. The protection diode 9 comprises a cathode 10 and an anode 11. The protection diode 9 serves to prevent damage of the RF power transistor 2 in case the voltage between collector 5 and base 3 increases to the breakdown level of the transistor. The protection diode 9 will clip at a lower level voltage V_{CE}, before breakdown of the transistor occurs.

The circuit 1 according to the present invention is produced in a standard double poly–silicon process for bipolar transistor devices, without the application of additional processing steps. The protection diode 9 is formed during the same processing steps as required for the power transistor 2.

Figure 2 shows schematically an exemplary layout in plane view for a device comprising a RF power transistor 2 and protection diode 9 according to the present invention. On the n-type epitaxial surface layer 13 of substrate 6 a base region 3, an emitter region 4, a collector region 12 and a protection diode region 9 are defined. In this layout at the surface level of the substrate 6, the base region 3 and emitter region 4 are located closely together in a common area. At some distance at the same surface level the diode region 9 is located. Below the surface level of the substrate 6, a buried collector region 12 is defined, which extends from below the base and emitter regions 3, 4 to below the diode region 9. In the collector region 12 a collector opening region 31 to connect the collector, is provided. Around these regions 3, 4, 5, 9, 31, a channel stopper (depicted by a dashed line) is defined to isolate the device from neighboring devices. Outside of the collector region 12 the channel stopper locally dopes the n-type epitaxial surface layer 13 into p-type. The lines AA' and BB' indicate the locations of the cross-sectional views as shown in Figures 3a-3m and Figures 4a, 4b respectively. It is noted that the buried collector region 12 may extend under a plurality of base and emitter regions 3, 4, that form, in a parallel connection, a single large power transistor. In that case, the channel stopper demarcates the area comprising this single large power transistor.

The processing steps required to form a circuit 1 according to the present invention are illustrated by the following Figures 3a–3m which schematically show a cross-sectional area, defined by the line AA' in Figure 2 wherein the power transistor 2 is formed in successive steps.

Figures 4a and 4b show a cross-sectional area of the protection diode 9, defined by the line BB' in Figure 2, in two respective preferred embodiments after the step of metallization.

Figure 3a shows a step F1 of the formation of a collector region. In substrate 6 a buried collector region 12 is formed. An implantation process defines a laterally confined n^+ region 12 in the p^- doped substrate 6 to form the collector 5. As known to persons skilled in the art, the collector region 12 may comprise several areas which are separated during their formation in this step F1 by means of a mask.

Figure 3b illustrates a step F2 of the formation of an n-type epitaxial silicon layer 13 on top of n^+ region 12. The dopant of n^+ region 12 diffuses slightly into layer 13 due to the thermal exposure during the deposition process of n-type epitaxial silicon layer 13.

Figure 3c illustrates a step F3 of lithographic formation of sacrificial masks 14, 15 that define the locations where in a later processing step base and emitter regions 3, 4 and a connection to the n^+ region 12 (collector 5) will be formed.

Figure 3d illustrates a step F4 of the implantation of dopant regions which define channel-stoppers 17, 18 in n-type epitaxial silicon layer 13.

Figure 3e shows a cross-sectional view after LOCOS oxidation in a step F5. In the n-type epitaxial silicon layer 13 oxidized regions 21 are formed using the sacrificial masks 14 and 15. The oxidized regions 21 isolate the areas 19, 20 to form, in a later processing step, base and emitter regions 3, 4 and a connection to the collector region 5, respectively. Due to thermal exposure during the LOCOS oxidation process, p-type dopant diffuses further into the substrate 6 extending the channel-stoppers 17 and 18 into the substrate 6.

In Figure 3f a step F6 of the formation of the connection to the collector region 5 (n^+ region 12) is illustrated. In the area 20 a deep n^+ doped plug 22 is defined by an implantation process. The plug 22 connects the n^+ region 12 to the surface of area 20.

Figure 3g illustrates a step F7 of the formation of the base and emitter regions 3, 4. A first p^{++} doped poly-silicon layer 23 is deposited, and subsequently patterned on area 19 using lithographic and etching steps as known in the art.

To provide passivation and isolation of the structure, in a next processing step F8 an oxide layer 24 is deposited on top of the structure, as shown in Figure 3h. By means of a masked etch using processing steps as known in the art, the emitter opening in layer 23 and 24 to area 19 is defined.

In Figure 3i a step F9 of the formation of nitride L-spacers 25 on the walls of the emitter opening is illustrated. During the formation of the L-spacers, p-type dopant (e.g. B) from the poly-silicon layer 23 diffuses into the n-type epitaxial silicon layer 13, forming a shallow p^+ doped region 26. By local implantation an implanted shallow p^+ doped region 26a is formed. Typically, the overall shallow p^+ doped region, comprising both region 26 and region 26a, has a length of 1-10 μm, a width of 0.3 μm and a depth of 0.2 – 0.25 μm. Also, by a local implantation step, a high doped n^+ region 50 is formed in the n-type epitaxial silicon layer 13 to provide a lower collector series resistance.

Figure 3j shows a step F10 of forming a poly-silicon layer and plug using processing steps as known in the art. A second poly-silicon layer 28 is deposited and subsequently patterned as the connection to the emitter region 4 of the transistor. By

diffusion of n-type dopant (e.g. As) from the poly-silicon layer 28, a very shallow n^+ doped region 27 is formed at the top of the implanted shallow p^+ doped region 26a.

Figure 3k shows a step F11 of forming the base region contact opening 29, 30 and the collector contact opening 31 by selective etching the oxide layer 24.

Finally, Figure 3l shows a step F12 of metallization, in which a metal layer is deposited on the structure. By a patterning step, metal connects 32, 33, 34, 35 are defined for connection to the base region 3 through the contact openings 29, 30, to the collector region 5 through contact opening 31, and to the emitter region 4 through poly-silicon plug 28, respectively.

Figure 3m shows schematically the cross-sectional view of the transistor part of the device to display the dopant regions 13, 26, 26a, 27 and 50, in closer detail. In Figure 3m, the base region 3, the emitter region 4, the n-type epitaxial silicon layer 13, the oxidized regions 21, the first p^{++} doped poly-silicon layers 23, the oxide layers 24, the nitride L-spacers 25, the shallow p^+ doped region 26, the implanted shallow p^+ doped region 26a, the very shallow n^+ doped region 27 and the highly doped n^+ region 50 are shown. Due to the geometry and the size of the contact area between the first p^{++} doped poly-silicon layer 23 and the n-type epitaxial silicon layer 13, a dopant profile for the shallow p^+ doped region 26 as schematically shown in Figure 3m, is created during the diffusion process. Also, due to the diffusion process, the shallow p^+ doped region 26, below the base region 3, has a concentration profile of p-type dopant that extends deeper than the concentration profile of p-type dopant in the implanted shallow p^+ doped region 26a below the emitter region 3.

Simultaneously with the transistor 2 the protection diode 9 is formed. This is accomplished by a selective use of separate steps in the aforementioned processing steps F1-F12 used to form the transistor.

Figure 4a shows a protection diode 9 according to the present invention after the step of metallization. It is made in the following way. In step F1, in the substrate 6 the n^+ region 12, formed as buried collector region 5 for the transistor, is extended laterally as the cathode region 10 of the protection diode 9. Subsequently, in step F2 the n-type epitaxial silicon layer 13 is deposited. Dopant from the n^+ region 12 diffuses slightly into the n-type epitaxial silicon layer 13 due to thermal exposure during epi growth. In step F3, a sacrificial mask is formed to define the area 41 where the anode 11 of the diode will be formed at a later stage. In step F4, a channel stopper 42 is formed. In step F5, oxidized regions 43 are formed using the LOCOS process to isolate the area of the anode 11. Due to annealing during the LOCOS process, the channel stopper 42 now extends into the substrate 6. In step F7, the first

p^{++} doped poly-silicon layer 23 is deposited and patterned as a p^{++} doped poly-silicon contact 44 on top of the area of the anode 11. Subsequently, in step F8 the oxide layer 24 for passivation and isolation is deposited over the p^{++} doped poly-silicon contact 44. Due to annealing during step F9, p-type dopant from the p^{++} doped poly-silicon contact 44 diffuses into the n-type epitaxial silicon layer to form a p-type doped region 45. In step F11, the oxide layer 24 is opened to create an anode contact opening. In metallization step F12, the anode contact opening is filled with metal 46.

In this preferred embodiment, the breakdown voltage level of the diode 9 is smaller than the breakdown voltage level between the base and the collector of the transistor, which is determined by the dopant profiles in the shallow p^+ doped region 26 and the p-type doped region 45, respectively, and their distances to the buried layer 12.

In the present invention, the area of the anode 11, as depicted by the p-type doped region 45, has typically a length of 1-10 μm, a width of 10 μm and a depth of 0.3 μm. Compared to the length and width of the combined shallow p^+ doped regions 26, 26a of the transistor as shown in Figure 3m (length: 1-10 μm, width: 0.3μm, depth: 0.2 – 0.25 μm), the areal size of the anode 11 of the diode 9 is much larger than the areal size of base and emitter regions 3, 4 of the transistor.

The difference in areal size influences the dopant profiles, in the shallow p^+ doped region 26 and the p-type doped region 45, as formed by the diffusion process. As known to persons skilled in the art, the kinetics of the dopant diffusion process in both the shallow p^+ doped region 26 and the p-type doped region 45 will be identical: the thermal exposure of the transistor 2 and diode 9 is identical during the processing steps F1-F12, the source material is identical for the transistor and diode areas: p-type dopant from the first p^{++} doped poly-silicon layer 23 and/or contact 44. The target material is also identical: n-type epitaxial silicon grown in the same process step F2.

However, the dopant profile below the larger p^{++} doped poly-silicon contact area 44 will extend slightly deeper into the n-type epitaxial silicon layer 13 due to a geometric effect: the dimensions of the dopant source as defined by the area 45 are larger. It is estimated that for a depth of the shallow p^+ doped region 26 of 0.2-0.25 μm, the depth of the p-type doped region 45 is 0.30 μm.

Also, since the kinetics of the dopant diffusion process in both the shallow p^+ doped region 26 and the p-type doped region 45 are identical, incidental process variations will influence the dopant profiles in both the shallow p^+ doped region 26 and the p-type doped region 45 in a similar way: the method to manufacture a protection diode according to

the present invention is self-defining. For example, if due to a higher annealing temperature in step F9, the diffusion depth for the dopant will be deeper for both the shallow p^+ doped region 26 and the p-type doped region 45, and all other things being equal, then the dopant profile of the p-type doped region 45 will still be the deeper one. Accordingly, the diode 9 will have a lower breakdown voltage than the base–collector transition of the transistor.

In devices comprising a transistor 2 and diode 9 according to the present invention, the breakdown voltage of the transistor between base and collector is 18 – 20 V, whereas the diode 9 has a breakdown voltage which is 2 V lower: 16 – 18 V.

The protection diode 9 comprises a capacitance which is present between the emitter 4 and collector 5, in parallel with the parasitic transistor capacitance 7. In order not to affect the efficiency of the transistor 2 too strongly, the capacitance of the diode 9 must be optimized by means of the areal size of the diode 9. A large capacitance of the diode 9 reduces the transistor efficiency as defined by the power added efficiency (the conversion from dc input power to RF output power). A small capacitance of the diode 9 results in a (too) small current flow through the diode 9, thus reducing the protection capability of the diode 9.

In a second preferred embodiment, the protection diode 9 may exhibit a still lower breakdown voltage. In Figure 4b the protection diode 9 is shown in this second preferred embodiment. The protection diode 9 according to the second embodiment is formed in the same way as explained above with reference to Figure 4a. Here, the channel stopper 42 as shown in Figure 4a, is replaced by a channel stopper 47 which in comparison to channel stopper 42, comprises a larger region extending under the p-type doped region 45 of the diode 9. All other parts of the diode structure shown in Figure 4b are identical to the ones shown in Figure 4a. Due to the extension of channel stopper 47 under the p-type doped region 45 of the diode 9, the breakdown voltage level is advantageously reduced to approximately 10V. However, due to the large size of the channel stopper 47, the capacitance of the protection diode 9 is strongly increased (with an increase in current flow and a reduction of the power added efficiency). By optimizing the channel stopper area 47, the breakdown voltage and the capacitance of the diode 9 can be tuned as required for the application of the device.

It will be appreciated that the method to manufacture a microelectronic device in a self-defining way is not restricted to the particular sequences of processing steps as described above. Other self-defining processing sequences, comprising the same technologies as above or others, may be conceivable. Also, the method is not limited to the described

device comprising a power transistor 2 and a protection diode 9, but may be applicable for other types of microelectronic devices as well. For example, the diode 9 may have a different function and may be used detached from the power transistor 2. In general, the method of the present invention may be used in a double poly-Si process for the formation of diodes comprising a junction from poly-silicon to monocrystalline silicon. For example, the method of the present invention may be used to manufacture, in one processing sequence, a plurality of such diodes with slightly different breakdown voltages, in dependence of the areal size of each of the diodes.

Moreover, the principle that the diffusion of dopant into a matrix layer from a covering feed layer is dependent on the geometry of the interface area between that matrix layer and the covering feed layer, can be applied to modify the diffusional transport of a dopant to proceed in one, two or three dimensions by proper definition of the actual size and shape of the interface area: differences in diffusion length in one dimension can be achieved as described above by varying the area size of the interface area. Two dimensional differences in diffusion can be obtained by using narrow lines with various size as the interface area. By using point contacts with various size as the interface area, even three dimensional differences in diffusion may be obtained.

CLAIMS:

1. A semiconductor arrangement comprising:

- a substrate having a substrate layer (13) with an upper surface and a lower surface, the substrate layer (13) being of a first conductivity type;
- a first buried layer (12) in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer (13), and a second buried layer (12) in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer (13);
- a first diffusion region (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer (12) for defining a first breakdown voltage between said first diffusion region (26) and said first buried layer (12);
- a second diffusion region (45) in said second portion of said substrate layer (13), being of said second conductivity type and having a second distance to said second buried layer (12) for defining a second breakdown voltage between said second diffusion region (45) and said second buried layer (12);

said first distance being larger than said second distance such that said first breakdown voltage is larger than said second breakdown voltage.

2. The arrangement according to claim 1, wherein said first diffusion region (26) is a base (3) of a bipolar transistor and said first buried layer (12) is a collector (5) of said bipolar transistor.

3. The arrangement according to claim 1 or 2, wherein said second diffusion region (45) is an anode of a protection diode (9) and said second buried layer (12) is a cathode of said protection diode (9).

4. The arrangement according to any of the preceding claims, wherein said first buried layer (12) is connected to said second buried layer (12), and said first and second buried layers (12) are manufactured in the same step.

5. The arrangement according to any of the preceding claims, further comprising a channel stopper region (42) in said second portion of said substrate layer (13); the channel stopper region (42) being of said first conductivity type, for electrically isolating said second portion of said substrate layer (13) within the substrate (6), wherein said channel stopper region (42) is arranged to extend substantially as an extended channel stopper region (47) in between said second diffusion region (45) and said second buried layer (12), for reducing said second breakdown voltage.

6. A method of manufacturing a semiconductor arrangement, comprising the steps of:

- providing a substrate with a substrate layer (13) with an upper surface and a lower surface, the substrate layer (13) being of a first conductivity type, a first buried layer (12) being provided in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer (13), and a second buried layer (12) being provided in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer (13);
- diffusing a first diffusion region (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer (12) for defining a first breakdown voltage between said first diffusion region (26) and said first buried layer (12);
- diffusing a second diffusion region (45) in said second portion of said substrate layer (13), being of said second conductivity type and having a second distance to said second buried layer (12) for defining a second breakdown voltage between said second diffusion region (26) and said second buried layer (12);

said first distance being larger than said second distance such that first breakdown voltage is larger than said second breakdown voltage.

7. A method according to claim 6, wherein said first and second diffusion regions (26, 45) are formed by depositing, in a single manufacturing step, a first poly-silicon layer (23) in a first area in said first portion and a second poly-silicon layer (44) in a second area in said second portion, and diffusing said first and second diffusion regions (26, 45) from said first and second poly-silicon layers (23, 44), respectively, in a single annealing step, said first area being smaller than said second area.

8. A method according to claims 6-7, further comprising the step of forming by ion-implantation a channel stopper region (42) in said second portion of said substrate layer (13); the channel stopper regions (42) being of said first conductivity type, for electrically isolating said second portion of said substrate layer (13) within the substrate (6) wherein said channel stopper region (42) is formed by ion-implantation as an extended channel stopper region (47) in between said second diffusion region (45) and said second buried layer (12), for reducing said second breakdown voltage.

ABSTRACT:

A semiconductor arrangement including:

- a substrate having a substrate layer (13) with an upper and lower surface, the substrate layer (13) being of a first conductivity type;
- a first buried layer (12) in the substrate, extending along said lower surface below a first portion of said upper surface of said substrate layer (13), and a second buried layer (12) in the substrate, extending along said lower surface below a second portion of said upper surface of said substrate layer (13);
- a first diffusion (26) in said first portion of said substrate layer (13), being of a second conductivity type opposite to said first conductivity type and having a first distance to said first buried layer (12) for defining a first breakdown voltage between said first diffusion (26) and said first buried layer (12);
- a second diffusion (45) in said second portion of said substrate layer (13), being of said second conductivity type and having a second distance to said second buried layer (12) for defining a second breakdown voltage between said second diffusion (45) and said second buried layer (12);

said first distance being larger than said second distance such that said first breakdown voltage is larger than said second breakdown voltage.

Fig.4a